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High Gain Operational Amplifier Design Using Positive Feedback and Current Distrubted Load

Vikrant Rawat, Hari Shanker Srivastava and Md. Mazharul Islam
Department of Electronic and Communication Engineering,
LNCT, Bhopal, (MP), India

(Corresponding author Vikrant Rawat)
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ABSTRACT: The paper represents low noise, high gain differential amplifier circuit using positive feedback at load and at differential end to increase gain.The circuit is designed with short-channel MOSFETs, low noise, and low voltage, resulting in DC gain amendment over a conventional CMOS diff-amp and commensurable to a kenned published diff-amp circuit.

Key words: Gain-enhancement, positive feedback, CMOS differential amplifier, distortion, op-amp.

I. INTRODUCTION

In scaled down CMOS advanced technology, short-channel contrivances pose many consequential challenges for analog and digital circuit designers [1- 4]. The challenges of designing high -performance circuits for analog and commixed signal often require trade-offs. The trade-off parameters include power dissipation, supply voltage, gain, speed, linearity, noise, and maximum voltage swings [1]. In designing CMOS amplifiers, perhaps the prominent challenge is reduced intrinsic gain of short channel contrivances [1-5], which is caused by reduced physical and electrical parameters and scaling inhibitions. The trend of impact with perpetuated contrivance scaling is only getting worse for future more minute MOSFETs and deep submicron contrivance generations.

Precision and high speed are often the two most paramount properties of analog and mixed-signal circuits. A wide variety of analog and commixed signal systems have performance that is limited by the settling deportment of a CMOS operational amplifier (Op- Amp). These include switched-capacitor filters. algorithmic A/D converters. sigma-delta converters. sample and hold circuits and pipeline A/D converters [l-3]. The settling demeanor of the Op-Amp determines tiles precision and the speed that can be reached. Conventional edifications designate expeditious settling requires single pole settling comportment and a high gain-bandwidth product (GBW) [l-2]. High precision withal requires a high DC gain. The low values of intrinsic transistor gain achieved by short-channel MOS contrivances utilized in high speed amplifiers has made it harder to get a high DC-gain from most subsisting amplifier architectures.

Most filters today are built with trans-conductance elements and capacitors [2] in integrator-predicated architectures. Building precise filters at high frequencies presents several challenges [8-9]. One major quandary is tlie phase error of the integrators [2, 4, 5]. The quality factors (Q) of the poles and zeros in the filter are highly sensitive to the phase of the integrator at tlie pole and zero frequencies. Filter performance is withal sensitive to the DC-gain of tlie integrators. A second challenge is to build an integrator with a sufficiently liigli DC-gain. These design challenges have been addressed in many publications including [1], [11]. Dynamic biasing of transconductance amplifiers has been proposed [4] as a method for enhancing gain and ameliorating settling. However. in the subsisting dynamically inequitable amplifiers. during the last part of settling period the DC gain will be very high but the current will be very low thus settling is slowed. Dynamically partial amplifiers have inhibited acceptance because of these disadvantages [8]. [9]. Moreover. a single-stage dynamically inequitable amplifier may not provide sufficient gain and cascading them is challenging [13]. Their speed is further circumscribed by the fact that the clock period must be long enough to ascertain the transfer of charge is adequately consummated in one cycle. Another amplifier design approach proposed for filter applications uses positive-feedback techniques to enhance the amplifier DC-gain without constraining its high frequency performance. This approach was considered by Laber and Gray. Nuata. and others [9-10].

Several techniques have been used to increment the DC-gain on diff-amps - cascading of gain stages, cascoding, and gain- enhancing [12].

This paper discusses a diff-amp circuit with gain-enhancing or gain-boosting technique utilizing positive feedback [6] - [10] The positive feedback circuit significantly increases the DC-gain of short-channel design, compared to a conventional CMOS diff-amp [1] - [4]. The DC-gain of the proposed diff-amp is additionally commensurable to a kenned published diff-amp circuit in [7].

This paper is organized as follows: Section II briefly shows a conventional CMOS diff-amp. Section III illustrates a kenned published diff-amp with positive feedback. Section IV presents an incipient gain-enhancement cross-coupled differential amplifier circuit with a positive feedback. Section V shows noise and distortion analyses of diff-amps. Section VI presents two operational amplifier circuits, which are designed with the new proposed diff-amp circuit described in this paper. Section VII shows simulation results for the op-amps. The conclusion is provided in Section VIII.

II. CONVENTIONAL CMOS DIFFERENTIAL AMPLIFIER

Fig. 1 shows a conventional CMOS fully differential diff--amp circuit [1] - [2]. The DC-gain of the circuit depends on the output resistance of both PMOS and NMOS transistors. The gain equation of the differential amplifier in Fig. 1 can be written as

$$|A_1V| = g_{\perp}(m1, 2)\ (r_1on\ ||r_{\perp}op\ )$$

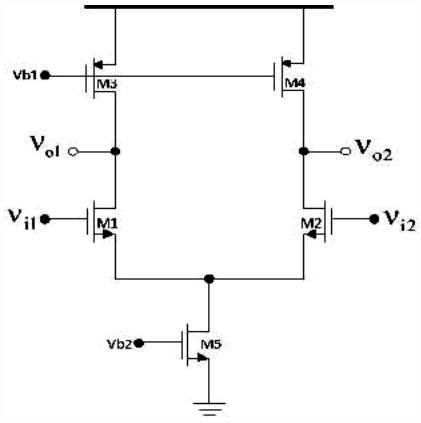

Fig. 1. A Conventional CMOS diff-amp circuit

III. KNOWN PUBLISHED DIFF -AMP CIRCUIT WITH POSITIVE FEEDBACK

Fig. 2 illustrates a known published diff-amp circuit using the positive feedback concept [7]. Without the cross-coupled active-load P-channel MOSFETs, the circuit behaves like the conventional CMOS diff-amp, shown in Fig. 1, and the DC- gain of the circuitis limited by the diode-connected MOSFETs .To achieve a very high gain, the circuit is equipped with the cross-coupled P-channel MOSFETs, which provide positive feedback and generate a negative transconductance $[" g] _{\perp} m$ "

The negative transconductance cancels some positive conductance at the output of the diff-amp circuit, and a very high gain is obtained.

Dc gain equation is :

$$A_d = \frac{-g_{m1}}{(g_{ds1} + g_{ds3} + g_{ds3c} + g_{m3} - g_{m3c})}$$

where $g_{ds1}, g_{ds3}, g_{ds3c}$ are the output conductance and gm1,gm3 and gm3c are the conductance of M1,M3,M3c respectively

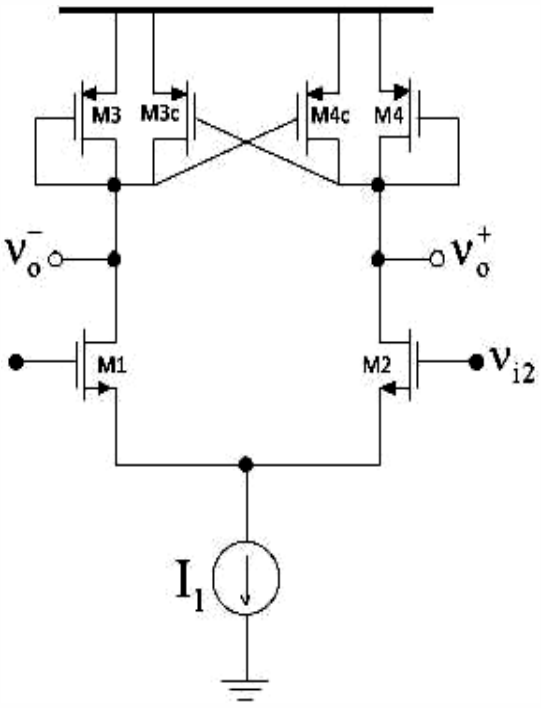

Fig. 2. differential amplifier with positive feedback at load

IV. GAIN-ENHANCEMENT DIFF-AMP UTILIZING POSTIVE FEEDBACK

Fig. 3 shows a configuration of diff-amp circuit utilizing positive feedback with integrated resistors. The circuit utilizes the same positive feedback concept as the kenned published diff-amp circuit illustrated in Fig. 2.

The circuit does not constrain the output voltage swing, due to the absence of the vertical stacking cascode structure or the MOSFET diode-connected circuit. The cross-coupled MOSFETs provide the positive feedback to the output nodes with a negative trans-conductance, -gm , which reduces the positive output resistance of both PMOS and NMOS loads of diff-pair circuit. As a result, the cross-coupled MOSFET increases the amplifier gain. The overall transfer function of diminutive-signal gain is indicted as

$$A_d = \frac{V_{O2} - V_{O1}}{V_{id}} = \frac{g_{m1}}{\left(\frac{1}{r_{01}} + \frac{1}{r_{02}} + \frac{1}{R_0} - G_m\right)}$$

where r01 and r02 are the output resistance of M1 and M3. The output resistance R0 can written as:

$$R_0 = \frac{v_t}{i_i} = r_{01c} + R + (g_{m1c} + g_{mb1c}).r_{01c}R$$

where g_{m1c}, g_{mb1c} and r_{01c} are the transconductance, body effect and output resistance, R is integrated resistor.

The transconductance G_m can also be written as

$$G_m = \frac{r_{01c}g_{m1c}}{r_{01c} + R + (g_{m1c} + g_{mb1c}).r_{01c}R}$$

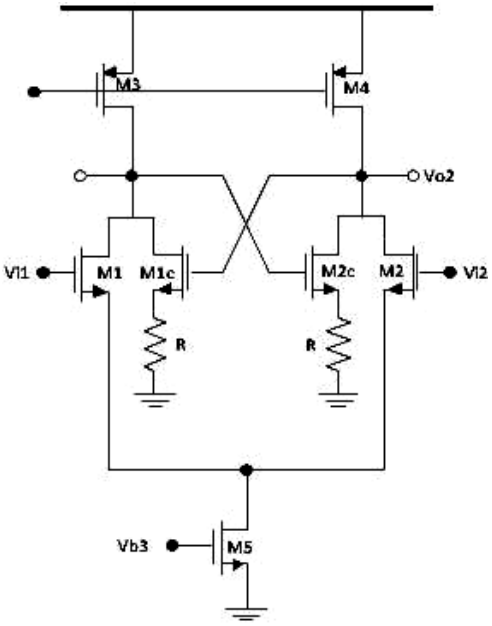

Fig 3. Differential amplifier with positive feedback at differential end using resistor.

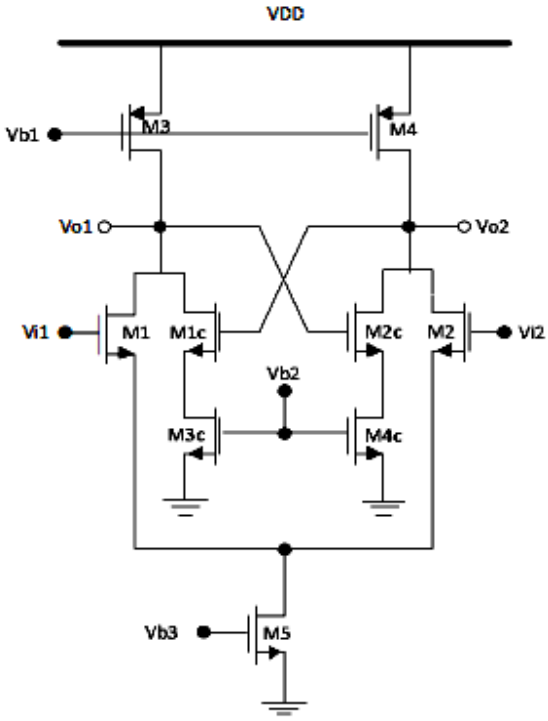

Fig. 4. Gain enhancement circuit using positive feedback at differential end using MOS.

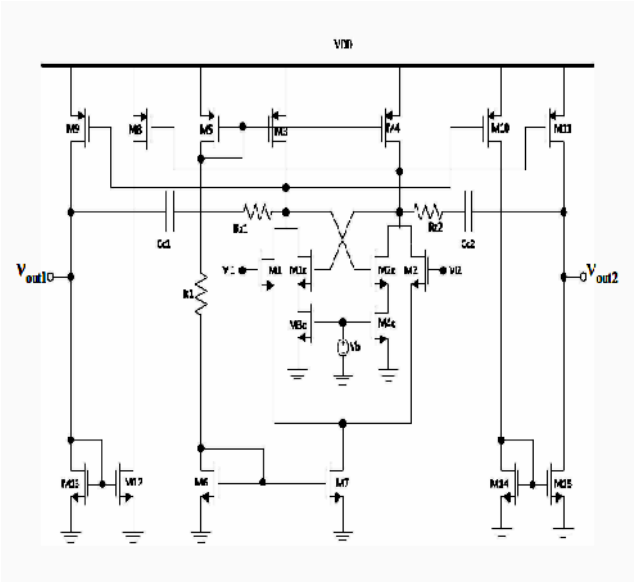

Fig. 5. Operational amplifier circuit with Positive feedback at differential end to increase the gain.

V. PROPOSED DIFFERENTIAL AMPLIFIER WITH ENHANCED GAIN

As diode connected load replaces the conventional resistance as it acquires large area on silicon chip, as shown in Fig 1, & Fig2 diode connected NMOS and PMOS load. The gain increase if we increase the load resistance, but it increase overdrive and hence the swing of output decreases,

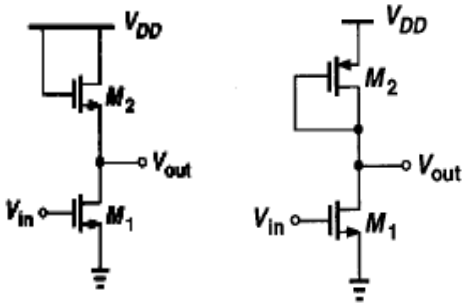

Fig. 6. CS stage with diode connected load, NMOS & PMOS.

$$A_V = -g_{m1}\frac{1}{g_{m2}+g_{mb2}}$$

$$= \frac{g_{m1}}{g_{m2}}\frac{1}{1+\eta}$$

$$\eta = \frac{g_{mb2}}{g_{m2}}$$

$$A_V = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}\quad\frac{1}{1+\eta}$$

if η is neglected the gain is independent of bias current and voltage, means the gain remains constant shows input and output varies linearly, to make it free from body effect we use PMOS as a active load.

As $I_{D1} = I_{D2}$ so,

$$\mu_n\left(\frac{W}{L}\right)_1 (v_{gs1}-v_{th1})^2 \approx \mu_p\left(\frac{W}{L}\right)_2 (v_{gs2}-v_{th2})^2$$

$$A_V \approx -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \cong A_V \approx -\left|\frac{v_{gs1}-v_{th1}}{v_{gs2}-v_{th2}}\right|$$

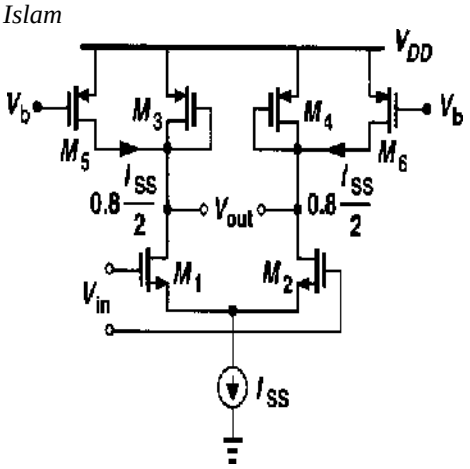

Fig. 7. Differential amplifier design using current distributed load to increase the gain.

In the circuit the diode-connected loads consume voltage headroom, thus creating a trade-off between the output voltage swings, the voltage gain, and the input CM range. For given bias current and input device dimensions, the circuit's gain and the PMOS overdrive voltage scale together. To achieve a higher gain, *(W /L)p* must decrease, thereby increasing $[VG_{s\,p} — V_{THp}]$ and lowering the CM level .

In order to alleviate the above difficulty, part of the bias currents of the input transistors can be provided by PMOS current sources. Illustrated in Fig. 4.33, the idea is to lower the g_m of the load devices by reducing their current rather than their aspect ratio. For example, if M5 and M6 carry 80% of the drain current of Ml and M2, the current through M3 and M4 is reduced by a factor of five. For a given I $V_{GSP} — V_{T\,H\,PI}$, this translates to a factor of five reduction in the trans-conductance of M3 and M4 because the aspect ratio of the devices can be lowered by the same factor. Thus, the differential gain is now approximately five times that of the case with no PMOS current sources. if M5 and M6 carry 80% of the drain current of Ml and M2, the current through M3 and M4 is reduced by a factor of five. For a given I $V_{GSP} — V_{THPI}$, this translates to a factor of five reduction in the transconductance of M3 and M4 because the aspect ratio of the devices can be lowered by the same factor. Thus, the differential gain is now approximately five times that of the case with no PMOS current sources. The above technique and positive feedback at differential pair is applied to increase the gain of operational amplifier, as shown in fig 8.

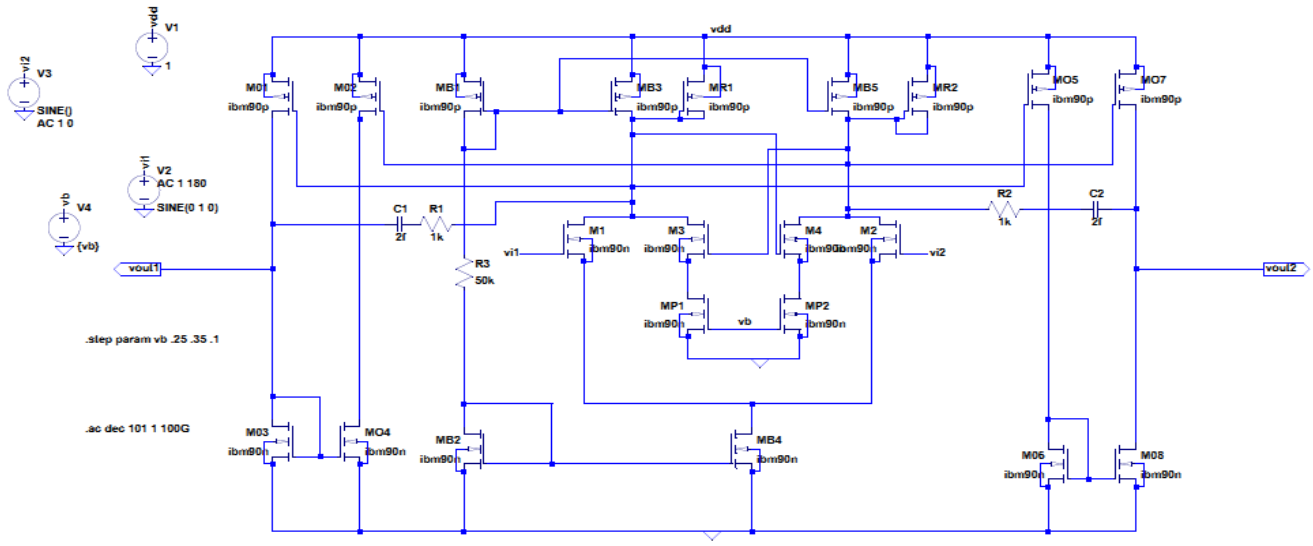

Fig. 8. Proposed Operational amplifier design using current distributed load and positive feed back at differential end to increase the gain.

The functionality of proposed buffer described as MB1-MB5 are used for biasing of differential NMOS, M01-M08 are used as output is stage of the proposed buffer, M3, M4, MP, MP2 are used as positive feedback to differential pair,M1 and M2 are used as differential pair input MR1, MR2 are used to enhance the gain of differential pair as described above , the value of Vb is set in between .25v to .35 volt to optimize the performance , the above differential amplifier designed with this specification of VDD =1v, DC gain = 100db, phase margin = 60° power dissipation 10 microwatts with unity gain frequency of 10 gigahertz at 27°C.

VI. NOISE ANALYSIS

In analog circuit design noise and distortion where unwanted signal which disturbs the normal operation of the circuit it actually degrades the quality of the signal which we get at output. For the conventional CMOS differential pair as shown in figure 1 the noise introduced by M1(NMOS) & M3 (PMOS) is given as:

$$+ \frac{2[(4kT\mu_{\downarrow}(eff,p))/(g_{\downarrow}pm'^2\ L_{\downarrow}(eclec,p)'^2\ )\ Q_{\downarrow}invp + K_{\downarrow}p/(C_{\downarrow}oxp\ w_{\downarrow}p\ L_{\downarrow}p\ )\ 1/f].g_{\downarrow}mp'^2\ (r_{\downarrow}on\ ||r_{\downarrow}op\ )'^2}{}$$

For our proposed circuit the differential half pair consist of M1, M3,MP1,MB3,MR1 the noise introduced by this circuit is analyzed as:

$$\overline{V^2_{noise,out}} = 2\frac{[(4kT\mu_{\downarrow}(eff,n))/(g_{\downarrow}m1'^2\ L_{\downarrow}(eclec,1)'^2\ )\ Q_{\downarrow}invn + K_{\downarrow}n/(C_{\downarrow}oxn\ w_{\downarrow}1\ L_{\downarrow}1\ )\ 1/f].g_{\downarrow}mn'^2\ (R_{\downarrow}c'^{=}\ )'^2}{+2[(4kT\mu_{\downarrow}(eff,n))/(g_{\downarrow}m3'^2\ L_{\downarrow}(eclec,3)'^2\ )\ Q_{\downarrow}invn + K_{\downarrow}n/(C_{\downarrow}oxn\ w_{\downarrow}3\ L_{\downarrow}3\ )\ 1/f].g_{\downarrow}mn'^2\ (R_{\downarrow}c'^{=}\ )'^2}$$
$$+2[(4kT\mu_{\downarrow}(eff,n))/(g_{\downarrow}mMP1'^2\ L_{\downarrow}(eclec,MP1)'^2\ )\ Q_{\downarrow}invn + K_{\downarrow}n/(C_{\downarrow}oxn\ w_{\downarrow}MP1\ L_{\downarrow}Mp1\ )\ 1/f].g_{\downarrow}mn'^2\ (R_{\downarrow}c'^{=}\ )'^2$$
$$+ \frac{+2[(4kT\mu_{\downarrow}(eff,p))/(g_{\downarrow}mMB3'^2\ L_{\downarrow}(eclec,MB3)'^2\ )\ Q_{\downarrow}invn + K_{\downarrow}n/(C_{\downarrow}oxn\ w_{\downarrow}MB3\ L_{\downarrow}MB3\ )\ 1/f].g_{\downarrow}mn'^2\ (R_{\downarrow}c'^{=}\ )'^2}{+v}$$
$$\frac{2[(4kT\mu_{\downarrow}(eff,p))/(g_{\downarrow}mMR1'^2\ L_{\downarrow}(eclec,MR1)'^2\ )\ Q_{\downarrow}invn + K_{\downarrow}n/(C_{\downarrow}oxn\ w_{\downarrow}MR1\ L_{\downarrow}MR1\ )\ 1/f].g_{\downarrow}mn'^2\ (R_{\downarrow}c'^{=}\ )'^2}{}$$

$$R_{\downarrow}C'^{=} = [1/r_{\downarrow}01\ + 1/r_{\downarrow}mb3''\ + (1 - g_{\downarrow}m3\ r_{\downarrow}o3)/(r_{\downarrow}13 + r_{\downarrow}mp1 + (g_{\downarrow}m3 + [gmb]_{\downarrow}m3)r_{\downarrow}m3\ r_{\downarrow}mp1\ )]$$

the $r_{\downarrow}mb3''$ is increased using current distributed load , as respect to r_{mb3} as stated above it is increased 5 times. So the noise in the proposed circuit will reduce with respect to differential amplifier without this current distributed load.

VII. SIMULATION RESULT

The operation amplifier circuit discuss about this design on 90 nm CMOS technology which is submitted in LT spies BSIM 4model. The above circuit gives significant improvement in the gain with reference to previous paper, as shown in fig 9 & fig 10, and noise analysis of proposed in fig 11, & 12 with respect to output 1 and output 2, a comparison chart is drawn in respect to supply voltage, power dissipation, DC gain, phase margin, unity gain frequency and noise.

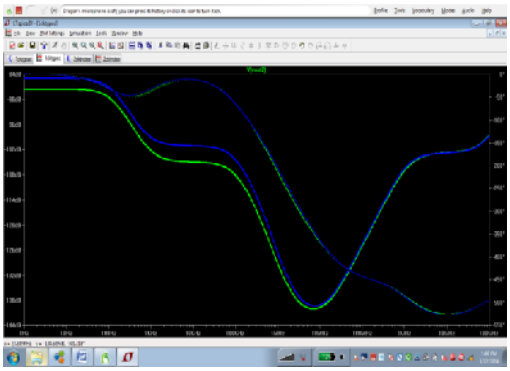

Fig. 9. Ac analysis of operational amplifier of ref [1].

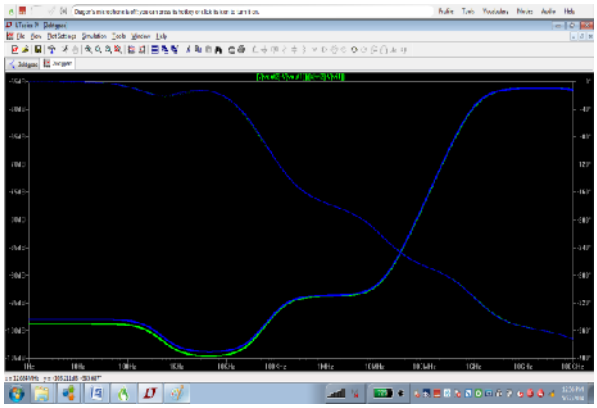

Fig. 10. Ac analysis of proposed operational amplifier.

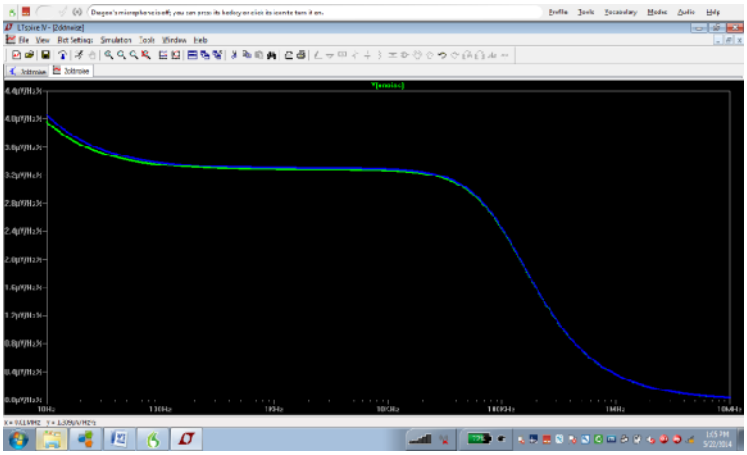

Fig. 11. Noise analysis of proposed operational amplifier.

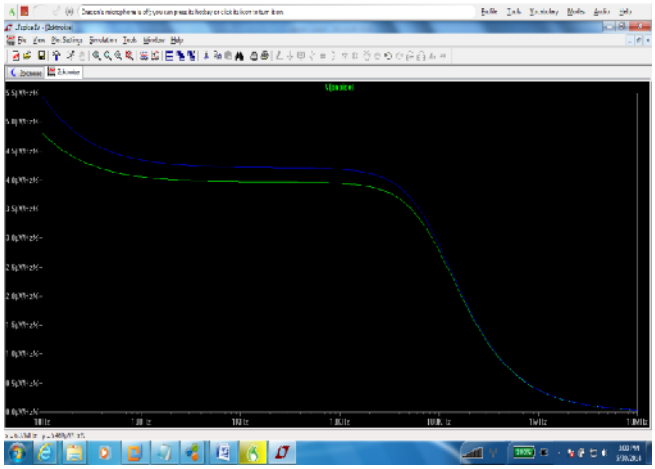

Fig. 12. Noise analysis of proposed operational amplifier.

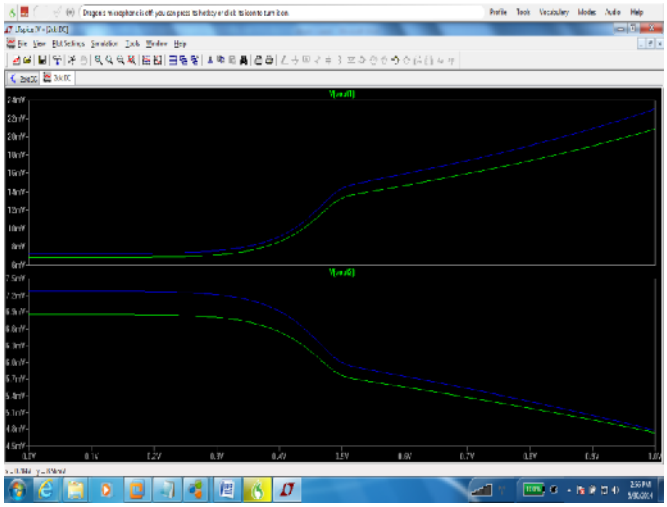

Fig. 13. DC analysis of proposed operational amplifier.

Table 1: Comparison table with previous work.

Circuit characteristics	Ref [1]	Ref [2]	Proposed work
Supply voltage	1V	1V	1V
Total current	111uA	NA	6µA
Power dissipation	NA	174µW	6µW
DC gain	83db	60db	95
Phase margin	60	107	60
Unity gain frequency	612M Hz	20.7GHz	700 Mhz
Noise at 10^0	223µv/ $hz^{\frac{1}{2}}$	92µv/ $hz^{\frac{1}{2}}$	3.6 µv/ $hz^{\frac{1}{2}}$

DESIGN PARAMETER

	(nm/nm)
M01,M02,M05,M07	**480/120**
M03,M04,M06,M08,MB1	**170/120**
MB2, MB4	**340/120**
MB3, MB5	**400/120**
MR1,MR2	**1700/120**
M1,M2	**170/120**
M3,M4	**180/180**
MP1,MP2	**150/120**

CONCLUSION

Positive feedback have significantly increase the Dc gain with respect to conventional differential amplifier. The simulation shows that the gain is improved and this gain is adjustable. The miller capacitance is added to increase the stability, to provide proper phase margin. As the positive feedback at load and diffrential end increases theDC gain 10 times approx, such types of diffrential amplifier were used in instrumentational amplifier.

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